## AMENDMENTS

**In the Claims**

1-20. (Canceled).

21. (Currently Amended) A method for simultaneously producing a gate feature and an interconnect feature in an integrated circuit ~~which have linewidths smaller than can be achieved by conventional methods~~, comprising:

(a) providing a substrate which is coated with a ~~positive tone~~ photoresist layer~~,~~;

(b) exposing said photoresist layer with a first mask comprised of alternating phase shift regions separated by chrome regions, to define shrunken gates;

(c) exposing said photoresist layer with a second mask comprised of attenuated phase shift regions ~~that define~~ defining interconnect features, chrome block regions ~~that protect~~ protecting shrunken gates ~~defined in the first exposure~~, and ~~clear~~ transparent regions~~,~~;

(d) developing said photoresist layer on said substrate to form a pattern~~,~~; and

(e) transferring the pattern formed in the photoresist layer through the ~~underlying~~ substrate with a dry etch process.

22. (Currently Amended) The method of claim 21 wherein the mask ~~substrate~~ is quartz or $CaF_2$, and an ~~the~~ exposing radiation of the exposing step is selected from one or more wavelengths in a range from about 150 nm to about 600 nm.

23. (Currently Amended) The method of claim ~~21~~ 22 wherein ~~the~~ linewidths in the ~~printed photoresist~~ pattern are between 1/4 and 1/2 of the ~~exposing wavelength~~ wavelengths in size.

24. (Original) The method of claim 21 wherein the substrate is polysilicon.

25. (Currently Amended) The method of claim 21 wherein from one to three ~~full-size~~ scattering bars are positioned between chrome lines that are used to define the shrunken gates on said ~~alternating phase shifting~~ second mask and each scattering bar separates a θ° phase region from a (180+θ)° phase region wherein θ is from 0 to 180.

26. (Currently Amended) The method of claim 25 wherein the width of said scattering bars is equal to or greater than the width of said chrome lines that define the shrunken gates and the phase widths of transparent regions adjacent to said chrome lines that define the shrunken gates are the same as the phase widths adjacent to said scattering bars.

27. (Currently Amended) The method of claim 21 wherein said attenuated phase shift regions are comprised of a half-tone material such as $MoSiO_xN_y$ which has been deposited on a transparent substrate.

28. (Currently Amended) The method of claim 27 wherein ~~the~~ said attenuated phase shift regions transmit from about 1% to 30% of incident light and phase shift said light by 180° relative to light that is transmitted through transparent regions that are not phase shifted.

29. (Currently Amended) The method of claim 27 wherein the attenuated phase shift regions contain from one to three scattering bars that are used to define a ~~smaller~~ interconnect feature ~~than is possible with conventional attenuated phase shifting~~.

30. (Currently Amended) The method of claim 29 wherein a ~~the~~ width of the scattering bars is between 33% and 100% of a width of the interconnect feature ~~width~~ and said scattering bars are separated from said interconnect by a distance that is from one to two times a ~~the~~ width of said interconnect.

31. (Original) The method of claim 21 wherein the exposed photoresist layer is developed with an aqueous base solution.

32. (Canceled).